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ELECTRONICS RESEARCH DIRECTORATE
AIR FORCE CAMBRIDGE RESEARCH LABORATORIES
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A NOTE ON SEMICONDUCTOR DEVICE FABRICATION

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ABSTRACT

This note presents a discussion of the basic steps in the making of germanium and silicon junction devices. It includes a list of the common etchants with their relation to various phases of device fabrication. Consideration is given to alloying for junctions and ohmic contacts, as well as information on applying the dopant alloy. Electroless nickel, electroless gold, furnace firing, and plating are examined in view of required modifications.

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INTRODUCTION

In order to make reproducible alloying devices from germanium and silicon, a careful control of all known parameters is required. In this control, one starts from the basic doping of the melt, through crystal pulling and orientation.[1,2,3] This report is written with the purpose of permitting fabrication of semiconductor devices of silicon or germanium with a minimum time loss, since construction of complicated equipment will not be involved.

Under these procedures, it is first assumed that the crystal has been properly doped, oriented to the (111) plane, sliced into wafers and diced. From this point on, the dice or slabs, and alloying material preparations are considered. The paper is limited specifically to techniques that may serve as a source of information to the engineer interested in device fabrication in laboratory quantities.

SURFACE PREPARATION

At the outset, it is assumed that the dice are properly oriented as concerns resistivity, crystal plane, minority carrier lifetime, etc. In order to reduce size, or to remove oxides that interfere with proper wetting, it becomes necessary to etch. The etches used are geared to the particular purpose required. They contain an oxidizing agent, in

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addition to an acid for removal of the formed oxide. The surfaces are removed by a process of oxidation and oxide removal. Some of the etches for germanium and silicon that have been found to work successfully are arranged in Table 1.

TABLE 1. ETCHES FOR GERMANIUM AND SILICON

I.	Acetic acid	240 cc			
	Nitric acid	400 cc	(Usually referred to as CP-4).		
	48% HF	240 cc			
	Bromine	5 cc			
II.		II-A	II-B	II-C	II-D*
	48% HF	1	1	1	1
	Nitric acid	1	1	3	0
	Water	3	0	0	0
III.	Hydrogen fluoride		1 part		
	Hydrogen peroxide		1 part		
	Water		4 parts		
IV.	Silver Etch				
	Hydrogen fluoride		40 cc		
	Nitric acid		20 cc		
	Water		40 cc		
	Silver nitrate		2 g		
V.	Bromine Etch				
	Hydrogen fluoride		30 cc		
	Nitric acid		40 cc	(Slightly modified CP-4.)	
	Acetic acid		30 cc		
	Bromine		0.6 cc		

*For oxide removal only.

The etches listed in Table 1 are among the most common. The choice of any group shown in this table is dependent upon etching rate required, in addition to the dopant present.[4]

In group V of the same table, iodine substituted for bromine works acceptably; this etch can be used to produce very smooth surfaces. Further, with addition of specified amounts of water, it can be used to give controlled etching rates.

Since halogens escape from the etching solutions described, it is important to make the preparation only as needed, or at least limit the shelf-standing time of the prepared solution. Again, emphasis is placed on the importance of temperature control and agitation during etching.

TABLE 2. CHARACTERISTICS OF ETCHING SOLUTIONS

Etch Number	Characteristics of Solution
II-A	Slow etch
II-B, III	Medium etch
I, II-C	Fast etch
II-D	Oxide removal
IV	Revelation of dislocation and etch pits in germanium
V	Rate etches
I	Polished surface

ELECTROLYTIC SURFACE ETCHING

Electrolytic stream etching is a technique developed to take advantage of surface tensions in confining the area of reaction. This method calls for the building of a jig for support of the device in a position

allowing (1) close proximity of the cathode, (2) control of etchant stream size, and (3) proper stream location on the device. With use of a 0.1 percent KOH solution, etching densities up to 10 amp/cm^2 for germanium have been satisfactory. One ampere per square centimeter appears to be the best current application, although much depends upon the resistivity, as well as the past history of the semiconductor. A better control over the amount of etch is obtained because the rate of electrolytic stream etching is slower.

ELECTROLYTIC ETCHING PROCEDURE

Electrolytic etching can be used on back biased silicon junctions to give controlled etching to the junction area. The diode (or transistor) is properly biased on a 10 percent solution of hydrofluoric acid, while a small amount of currentis passed through the device. Good regulation is maintained by controlling the solution temperature and the applied current.

SURFACE PREPARATION OF ALLOYS

To remove oxide layers, the dice are etched; this is followed by alloying which must take place before the formation of a new oxide layer. Metals used for alloying, ohmic or rectifying, should also be surface treated. Table 3 lists chemicals and composition that will accomplish the required surface preparation of the alloys.

TABLE 3. SURFACE PREPARATION OF ALLOYS

MATERIAL	COMPOSITION (ratios unless specified)						
	Lead and Lead Alloys	Gold and Silver	Lead and Lead Alloys	Aluminum	Aluminum	Nickel	Tin
Acetic acid	3						50
Hydrofluoric acid				1	10		
Nitric acid				1	50		
Fluoboric acid			5				
Hydrochloric acid						1	
Hydrogen peroxide	1						2 drops
Sodium cyanide		5					
Sodium nitrite		5					
Water		90	95	98	40	2	50

ALLOYING PROCEDURE

With the oxide removed, or at least limited, from both the semiconductor and the alloy metal, alignment in close proximity and confinement processes are considered. In order not to introduce unwanted additional donors or acceptors, extreme care should be exercised in the selection of the boat material, as well as in the cleanliness of the gaseous ambients. Hydrogen is commonly used to provide an inert atmosphere and, simultaneously, to remove oxide at elevated temperatures. The removal of oxides in some instances is given an assist through the use of hydrazine fluxes in the 300° to 400°C range and of titanium hydride at 950°C.

During alloying, the semiconductor is dissolved in the metal at a given temperature; it is then allowed to recrystallize onto the bulk semiconductor. With the action, a crystal structure is built embodying the atoms of the metal into the silicon crystal; this is done under influence of the phase diagram. In the process, the amount of impurity retained in solid solution varies in accordance with the segregation principle[6]

$$N(x) = kNo(1-g)^{k-1},$$

where

$N(x)$ = the impurity density at any distance x,

No = the original concentration of solute in the liquid,

k = segregation coefficient ratio $\frac{\text{imp in sol}}{\text{imp in liq}}$ at interface,

g = fraction of the original volume which has solidified.

This same principle is employed in meltback transistor zone refining.

Thermal mismatch, caused by the different coefficients of expansion of components, tends to destroy the interface contacts, ohmic and rectifying. By specific use of alloy composition, such as employing softer metals that will absorb the strain, or using alloys that will not become brittle upon cooling, as well as proper temperature cycling, thermal mismatch will be minimized.

REQUIRED CHARACTERISTICS FOR DEVICE PERFECTION

The following required characteristics are noteworthy:

1. Flat parallel junctions. - Flat parallel junctions are important for uniformity of characteristics and for width control of the base region. As previously stated, the area of penetration is determined by the alloying temperature, dot volume (according to the phase diagram), and the wettability of the semiconductor dot. The dot volume and wetted area are so chosen that the wetting angle between the semiconductor and dot limits spreading, owing to liquid forces.

2. Dot penetration control. - Forces and procedures for the control of dot penetration are:

a. Temperature.

b. Addition of a metal to the dot, as an oxygen getter.

c. Addition of a metal as a reducer of surface tension.

d. Alloy combination for reduction of solubility in semiconductors; e.g., addition of lead.

e. Addition of semiconductor to the alloy, as limiter of amount needed for saturation.

f. Intermediate metal to wet the semiconductor; in turn, soluble in the carrier alloy.

g. Soft metal to compensate for thermal mismatch.

3. Cooling effect. - The cooling effect is critical. Accordingly, it must be slow enough for equilibrium to take place. Since cooling rates under equilibrium conditions, or conditions closely approaching equilibrium, must be infinitely slow, they are seldom if ever attained in practice. Therefore, if the alloy solidifies before the composition of the crystals can be equalized through diffusion, each crystalline section will be composed of successive doping concentrates. If an eutectic exists and the temperature is held constant for a long enough time during the cooling cycle at the eutectic, diffusion will cause the composition to be more uniform, and the concentration will approach the reported solidus. Strain gradients accompany the concentration gradients.

In reducing thermal mismatch, a cooling rate of 3° to 5° per minute has been found effective. The addition of tin or lead also has been

effective in this direction. However, there is the disadvantage of lowering the alloy melting point.

4. Temperature cycling. - In order to take advantage of temperature cycling, the following three procedures are considered:

a. Increase furnace temperature gradually; hold; decrease gradually.

b. Increase to wetting temperature gradually; hold; increase to temperature established for depth penetration; decrease gradually.

c. Heat, first, to penetration temperature; hold; second, reduce to slightly above eutectic temperature; then decrease gradually.

For alloying below 600°C and for tabbing operations, the first procedure is satisfactory; for alloying above 600°C, the second and third are recommended. For maximum uniformity, the second approach is best. Nevertheless, in the laboratory, the third method is the most frequently used. To compensate for the "wetting temperature step," pressure is applied to the alloy. This keeps the alloy dot in close proximity to the semiconductor, tending to force out the oxide layer from between the two components. It also acts against the surface tension effect of the alloy, resulting in better wettability.

Bonding which is truly ohmic can be obtained by means of the techniques presented.

MECHANICAL BONDING PROCEDURES

Description follows of several methods:

1. Vacuum type. - This approach consists in depositing various metals and alloys upon the surface of the semiconductor. A subsequent heat treatment followed by a redeposit, or a heat treatment during deposit will give the required bonding mechanically and electrically.

2. Liquid plating. - The method requires placing the semiconductor in the proper liquid solutions. A metallic deposit is then placed upon the material either by a chemical reaction or an applied field. Two effective divisions are:

a. Electroless nickel plating.

b. Electroless gold plating.

Variations exist in electroless nickel plating. With equipment consisting of a heating mantle, Variac, and a thermometer, the described procedure has been successfully followed in the Electronic Material Sciences Laboratory.

First, the solution is made by adding

nickel chloride, $NiCl_2 6H_2O$	30 g
sodium ortho-phosphate dihydride, $NaH_2PO_2H_2O$	10 g
dibasic ammonium citrate, $(NH_4)_2HC_6H_5O_7$	65 g
ammonium chloride, NH_4Cl	50 g

to a liter of water. Ammonium hydroxide (NH_4OH) is then added until a dark blue color appears.[1]

During the plating process, ammonium hydroxide escapes. Consequently, additional amounts are necessary for blue color preservation.

Good results have been obtained by use of a water-cooled condenser that returns the escaping gas to the solution. Heated to 95°C, the solution is maintained at that temperature.

The semiconductor sample is prepared by dissolving the oxide layer in 48 percent hydrogen fluoride (HF). Without rinsing, it is placed in the electroless nickel solution. Plating time is arbitrarily taken as 4 minutes. No soldering attempts on a surface of this type should be made. However, an alloying at 700°C for one minute, in addition to a replating, will give the desired results.

In electroless gold plating, a process for depositing gold on silicon, the following procedure is outlined:

First, remove the oxide surface of the silicon, and simultaneously activate the surface by use of a solution of potassium fluoride (KF) and potassium hydroxide (KOH). Second, place the silicon into a solution prepared as follows:

potassium fluoride (hydrated), $KF\text{-}2H_2O$	100 g
potassium hydroxide, KOH	100 g
Dilute to one liter.	
Add potassium auric cyanide, $KAu(CN)_2$ to saturation.	

Electroless gold plating is accomplished most satisfactorily at 50°C. As in electroless nickel plating, the plated silicon should be alloyed. For the latter, a temperature of 400°C, which is above the

gold silicon eutectic, has proved adequate. Firing time is approximately 10 minutes.

CONCLUSIONS

The report presents device fabrication methods used in this laboratory. Basically described, the procedures outlined are primarily related to experimental studies. Modification of the techniques is essential in meeting particular requirements; for example, in construction of tunnel diodes, the diffusion of impurities must present a sharp gradient. Accordingly, heat treatments are to be avoided. Directly opposed is the slow annealing used in so-called rectifier diodes. Resistivity, lifetime, junction width, surface type, and other parameters controlling the device will determine the modification for a precise technique. Cleanliness is of major emphasis; purest reagents and ambient control are imperative.

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